That which is claimed is:

1. An electronic device comprising:

a first electronic substrate;

a second electronic substrate on the first electronic substrate;

a third electronic substrate on the second electronic substrate wherein the second electronic substrate is between the first and third electronic substrates;

a first electrical and mechanical connection between the first and third electronic substrates wherein the first electrical and mechanical connection bypasses the second substrate; and

a second electrical and mechanical connection between the second and third electronic substrates.

2. An electronic device according to Claim 1 wherein the second electronic substrate is offset relative to the first and third electronic substrates so that the first and third electronic substrates extend beyond an end of the second electronic substrate.

3. An electronic device according to Claim 2 wherein the first electrical and mechanical connection is between portions of the first and third electronic substrates extending beyond the end of the second electronic substrate.

4. An electronic device according to Claim 3 further comprising:

a conductive trace on a surface of the third electronic substrate, the conductive trace providing an electrical coupling between the first and second electrical and mechanical connections.

5. An electronic device according to Claim 1 further comprising:

a third electrical and mechanical connection between the first and second electronic substrates.

6. An electronic device according to Claim 5 further comprising:

a conductive trace on a surface of the first electronic substrate, the conductive trace providing an electrical coupling between the first and third electrical and mechanical connections.

7. An electronic device according to Claim 1 wherein the first electrical and mechanical connection comprises a first conductive bump between the first and third electronic substrates and wherein the second electrical and mechanical connection comprises a second conductive bump between the second and third electronic substrates.

8. An electronic device according to Claim 7 wherein the first conductive bump has a greater volume than the second conductive bump.

9. An electronic device according to Claim 1 wherein each of the first and third electronic substrates includes a device side having electronic circuits thereon and a backside, wherein a backside of the first electronic substrate is adjacent the second electronic substrate and wherein a device side of the third electronic substrate is adjacent the second electronic substrate.

10. An electronic device according to Claim 9 wherein both of the first and third electronic substrates are memory devices.

11. An electronic device according to Claim 10 wherein both of the first and second electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the third electronic substrate.

12. An electronic device according to Claim 11 wherein the second electronic substrate comprises a memory device.

13. An electronic device according to Claim 12 wherein both of the first and second electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the second electronic substrate, and to a data input, a data output, and/or an address input of the first electronic substrate.

14. An electronic device according to Claim 10 wherein the first and third electronic substrates comprise memory devices having a same layout.

15. An electronic device according to Claim 1 further comprising:

a printed circuit board, wherein the first and third electronic substrates comprises integrated circuit device substrates having devices sides facing the printed circuit board and backsides facing away from the printed circuit board;

a third electrical and mechanical connection between the first electronic substrate and the printed circuit board;

a fourth electrical and mechanical connection between the second electronic substrate and the printed circuit board; and

a fifth electrical and mechanical connection between the second electronic substrate and the first electronic substrate.

16. An electronic device according to Claim 15 wherein the printed circuit board includes a first conductive pad to which the third electrical and mechanical connection is bonded and a second conductive pad to which the fourth electrical and mechanical connection is bonded, wherein the first conductive pad has a greater surface area than the second conductive pad.

17. An electronic device according to Claim 15 further comprising:

a first conductive trace on the printed circuit board providing electrical coupling between the third and fourth electrical and mechanical connections;

a second conductive trace on the second electronic substrate providing electrical coupling between the fourth and fifth electrical and mechanical connections; and

a third conductive trace on the first electronic substrate providing electrical coupling between the fifth and first electrical and mechanical connections.

18. An electronic device according to Claim 17 wherein the first and third electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the first electronic substrate, and wherein the first and third electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the third electronic substrate.

19. An electronic device according to Claim 1 further comprising:

a fourth electronic substrate on the third electronic substrate so that the third electronic substrate is between the second and fourth electronic substrates;

a fifth electronic substrate on the fourth electronic substrate so that the fourth electronic substrate is between the third and fifth electronic substrates;

a third electrical and mechanical connection between the second and fourth electronic substrates;

a fourth electrical and mechanical connection between the fourth and third electronic substrates; and

a fifth electrical and mechanical connection between the third and fifth electronic substrates;

wherein the first, second, third, fourth and fifth electrical and mechanical connections comprise portions of a signal path, wherein an electrical coupling is provided between the signal path and an electronic circuit of the fifth electronic substrate, and wherein the signal path is free of electrical coupling with an electronic circuit of the third electronic substrate.

20. An electronic device according to Claim 1 further comprising:

a heat dissipating layer between the first and second electronic substrates, wherein the heat dissipating layer includes a material that is thermally conductive.

21. An electronic device comprising:

a printed circuit board;

a first electronic substrate on the printed circuit board;

a second electronic substrate on the first electronic substrate wherein the first electronic substrate is between the printed circuit board and the second electronic substrate; and

a third electronic substrate on the second electronic substrate wherein the second electronic substrate is between the first and third electronic substrates, wherein the second electronic substrate is offset relative to the first and third electronic substrates so that the first and third electronic substrates extend beyond an end of the second electronic substrate.

22. An electronic device according to Claim 21 further comprising:

a first electrical and mechanical connection between the first and third electronic substrates; and

a second electrical and mechanical connection between the second and third electronic substrates.

23. An electronic device according to Claim 22 wherein the first electrical and mechanical connection is between portions of the first and third electronic substrates extending beyond the end of the second electronic substrate.

24. An electronic device according to Claim 22 further comprising:

a conductive trace on a surface of the third electronic substrate, the conductive trace providing an electrical coupling between the first and second electrical and mechanical connections.

25. An electronic device according to Claim 22 further comprising:

a third electrical and mechanical connection between the first and second electronic substrates.

26. An electronic device according to Claim 25 further comprising:

a conductive trace on a surface of the first electronic substrate, the conductive trace providing an electrical coupling between the first and third electrical and mechanical connections.

27. An electronic device according to Claim 21 wherein the first electrical and mechanical connection comprises a first conductive bump between the first and third electronic substrates and wherein the second electrical and mechanical connection comprises a second conductive bump between the second and third electronic substrates.

28. An electronic device according to Claim 27 wherein the first conductive bump has a greater volume than the second conductive bump.

29. An electronic device according to Claim 21 wherein each of the first and third electronic substrates includes a device side having electronic circuits thereon and a backside, wherein a backside of the first electronic substrate is adjacent the second electronic substrate and wherein a device side of the third electronic substrate is adjacent the second electronic substrate.

30. An electronic device according to Claim 29 wherein both of the first and third electronic substrates are memory devices.

31. An electronic device according to Claim 30 further comprising:

a first electrical and mechanical connection between the first and third electronic substrates; and

a second electrical and mechanical connection between the second and third electronic substrates, wherein both of the first and second electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the third electronic substrate.

32. An electronic device according to Claim 31 wherein the second electronic substrate comprises a memory device.

33. An electronic device according to Claim 32 wherein both of the first and second electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the second electronic substrate, and to a data input, a data output, and/or an address input of the first electronic substrate.

34. An electronic device according to Claim 30 wherein the first and third electronic substrates comprise memory devices having a same layout.

35. An electronic device according to Claim 21 wherein a second end of the second electronic substrate extends beyond the first and third electronic substrates.

36. An electronic device according to Claim 35 wherein the first and third electronic substrates comprises integrated circuit device substrates having devices sides facing the printed circuit board and backsides facing away from the printed circuit board, the electronic device further comprising:

a first electrical and mechanical connection between the first and third electronic substrates;

a second electrical and mechanical connection between the second and third electronic substrates;

a third electrical and mechanical connection between the first electronic substrate and the printed circuit board;

a fourth electrical and mechanical connection between the second electronic substrate and the printed circuit board; and

a fifth electrical and mechanical connection between the second electronic substrate and the first electronic substrate.

37. An electronic device according to Claim 36 wherein the printed circuit board includes a first conductive pad to which the third electrical and mechanical connection is bonded and a second conductive pad to which the fourth electrical and mechanical connection is bonded, wherein the first conductive pad has a greater surface area than the second conductive pad.

38. An electronic device according to Claim 36 further comprising:

a first conductive trace on the printed circuit board providing electrical coupling between the third and fourth electrical and mechanical connections;

a second conductive trace on the second electronic substrate providing electrical coupling between the fourth and fifth electrical and mechanical connections; and

a third conductive trace on the first electronic substrate providing electrical coupling between the fifth and first electrical and mechanical connections.

39. An electronic device according to Claim 38 wherein the first and third electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the first electronic substrate, and wherein the first and third electrical and mechanical connections are electrically coupled to a data input, a data output, and/or an address input of the third electronic substrate.

40. An electronic device according to Claim 35 further comprising:

a fourth electronic substrate on the third electronic substrate wherein the third electronic substrate is between the second and fourth electronic substrates;

a fifth electronic substrate on the fourth electronic substrate wherein the fourth electronic substrate is between the third and fifth electronic substrates, wherein the fourth electronic substrate is offset relative to the first, third, and fifth electronic substrates so that the second end of the second electronic substrate extends beyond the first, third, and fifth electronic substrates, and so that the first, third, and fifth electronic substrates extend beyond the fourth electronic substrate.

41. An electronic device according to Claim 21 further comprising:

a heat dissipating layer between the first and second electronic substrates wherein the heat dissipating layer includes a material that is thermally conductive.

42. An electronic device comprising:

a first electronic substrate having opposing first and second surfaces;

a second electronic substrate on the first electronic substrate, the second electronic substrate having opposing first and second surfaces;

a third electronic substrate on the second electronic substrate, the third electronic substrate having opposing first and second surfaces, wherein the second electronic substrate is between the first and third electronic substrates; and

a signal path extending along the first surface of the second electronic substrate, to the second surface of the first electronic substrate, along the second surface of the first electronic substrate, to the first surface of the third electronic substrate, along the first surface of the third electronic substrate, and to the second surface of the second electronic substrate.

43. An electronic device according to Claim 42 wherein the signal path comprises a first conductive trace on the first surface of the second electronic substrate, a first electrical and mechanical connection between the first surface of the second electronic substrate and the second surface of the first electronic substrate, a second conductive trace on the second surface of the first electronic substrate, a second electrical and mechanical connection between the second surface of the first electronic substrate and the first surface of the third electronic substrate, a third conductive trace of the first surface of the third electronic substrate, and a third electrical and mechanical connection between the first surface of the third electronic substrate and the second surface of the second electronic substrate.

44. An electronic device according to Claim 43 wherein the first, second, and third electrical and mechanical connections comprise respective conductive bumps.

45. An electronic device according to Claim 42 wherein the first and third electronic substrates comprise integrated circuit devices, wherein the first side of the first and third electronic substrates comprises a device side and wherein the second side of the first and third electronic substrates comprises a backside.

46. An electronic device according to Claim 45 wherein the signal path is electrically coupled to an electronic circuit of the third electronic substrate.

47. An electronic device according to Claim 45 wherein the second electronic substrate comprises an integrated circuit device, wherein the first side of the second electronic substrate comprises a device side and wherein the second side of the second electronic substrate comprises a backside.

48. An electronic device according to Claim 47 wherein the signal path is electrically coupled to an electronic circuit of the second electronic substrate and to an electronic circuit of the third electronic substrate.

49. An electronic device according to Claim 47 wherein the first, second, and third electronic substrates comprise respective memory devices.

50. An electronic device according to Claim 42 further comprising:

a fourth electronic substrate on the third electronic substrate wherein the third electronic substrate is between the second and fourth electronic substrates; and

wherein the signal path further extends along the second surface of the second electronic substrate, and to a first surface of the fourth electronic substrate.

51. An electronic device according to Claim 50 wherein the signal path is electrically coupled with electronic circuits of the second and fourth substrates.

52. An electronic device according to Claim 50 wherein the signal path is electrically coupled with an electronic circuit of the fourth electronic substrate, and wherein the signal path is free of electrical coupling with an electronic circuit of the second electronic substrate.

53. An electronic device according to Claim 42 further comprising:

a heat dissipating layer between the first and second electronic substrates, the heat dissipating layer comprising a material that is thermally conductive.

54. An electronic device comprising:

a substrate having opposing first and second surfaces;

a first array of interconnection structures on the first surface of the substrate wherein the first array of interconnection structures are arranged in a first pattern;

a second array of interconnection structures on the second surface of the substrate wherein the second array of interconnection structures are arranged in a second pattern and wherein the second pattern is a mirror image of the first pattern.

55. An electronic device according to Claim 54 wherein the first array of interconnection structures comprises an array of interconnection bumps and wherein the second array of interconnection structures comprises an array of conductive pads free of interconnection bumps.

56. An electronic device according to Claim 55 wherein the interconnection bumps comprise solder bumps and wherein the conductive pads comprise solder wettable pads.

57. An electronic device according to Claim 54 further comprising:

a third array of interconnection structures on the first surface of the substrate spaced apart from the first array of interconnection structures wherein the third array of interconnection structures are arranged in a third pattern;

a fourth array of interconnection structures on the second surface of the substrate spaced apart from the second array of interconnection structures wherein the fourth array of interconnection structures are arranged in a fourth pattern, wherein the fourth pattern is a mirror image of the third pattern.

58. An electronic device according to Claim 57 further comprising:

a first plurality of conductive traces on the first surface of the substrate wherein the first plurality of conductive traces provide interconnection between at least some of the interconnection structures of the first and second arrays on a one to one basis.

59. An electronic device according to Claim 54 wherein the substrate comprises an integrated circuit substrate such that the first surface is a device side of the substrate having electronic circuits thereon and the second surface is a backside of the substrate.

60. An electronic device according to Claim 59 wherein the integrated circuit device comprises an integrated circuit memory device.

61. An electronic device comprising:

a first integrated circuit substrate;

a second integrated circuit substrate mounted on the first integrated circuit substrate;

a third integrated circuit substrate mounted on the second integrated circuit substrate such that the second integrated circuit substrate is between the first and second integrated circuit substrates;

at least one large bump providing electrical and mechanical connection between the first and third integrated circuit substrates; and

at least one small bump providing electrical and mechanical connection between the second and third integrated circuit substrates wherein the at least one large bump has a greater volume than the at least one small bump.